ABSTRACT

A circuit for interfacing between a first component 11 operating at a first clock rate and a second component 12 operating at a second clock rate, wherein the second clock rate is higher than the first clock rate. The circuit comprises a first buffer 13 coupled to the first component 11; a second buffer 14 coupled to the second component 12; and a copy/access controller 15, 16, 17 connected to the first buffer 13, the second buffer 14, and the second component 12. The copy/access controller 15, 16, 17 is operable to copy data from the first buffer 13 to the second buffer 14 when the first buffer 13 is substantially full. It is also operable to prompt the second component 12 to access the second buffer 14 when the data is copied from the first buffer 13. The buffers can be random access memories or shift registers, and can be integrated onto the same semiconductor die as either the first or second component.